REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The features of independent Claim 1 have been incorporated into Claims 2 and 11. The term "ONO layer" from Claim 1 and in Claims 9 and 10, has been changed to "ONO stack". This change is made neither for patentability reasons nor for narrowing the scope of the claim but made solely to more distinctly claim the invention. Support for this amendment is found in the Specification. (See page 4, line 3.) No new matter is added.

35 U.S.C. § 102(e) - ANTICIPATION

The Examiner rejected Claims 1 and 20-25under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,319,775 ("Halliyal"). The Examiner states:

Claims 1 and 20-25 are canceled.

35 U.S.C. § 103(a) - OBVIOUSNESS

The Examiner rejected Claims 1-21, 24 and 25 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,836,772 ("Chang") in view of "Electrical Properties of Composite Gate Oxides Formed by Rapid Thermal Processing," IEEE Transactions on Electron Devices, April 1996, by Misra et al. ("Misra"). The Examiner states:

> Chang et al. show all aspects of the instant invention (e.g. Figure 1 and Column 5 Lines 29 to 35) including:
>
> - forming a second silicon dioxide layer 16 by thermally depositing said second silicon dioxide layer on a silicon nitride layer 14
> - all part of a EEPROM flash memory device (Column 4 Lines 24 to 27)

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Chang et al. do not show the annealing of the ONO layer in a batch furnace or a Rapid Thermal Annealing tool using NO or N_20 in the gas mixtures claimed and using argon, nitrogen and/or oxygen as carrier gases or using RTCVD for forming said second silicon dioxide layer. Misra et al. teach (Section IIIC. EFFECT OF POST-DEPOSITION ANNEALING Pages 640 to 642) to use either a batch furnace or a Rapid Themal Annealing tool using N0 or N_20 in the gas mixtures claimed and to use argon, nitrogen and/or oxygen as carrier gases and to use RTCVD for forming silicon dioxide layers (Section II EXPERIMENT Page 637) to improve the quality of the oxides (Section V. Conclusion Page 645). It would have been obvious to a person ordinary skill in the art at the time of invention to use either a batch furnace or a Rapid Thermal Annealing tool using NO or N_20 in the gas mixtures claimed and to use argon, nitrogen and/or oxygen as carrier gases and to use RTCVD for forming silicon dioxide layers as taught by Misra et al. in the process of Chang et al. to improve the quality of the silicon dioxide.

INSUFFICIENT MOTIVATION TO COMBINE

Applicant believes the Examiner is improperly using hindsight in light of the present claims to combine and modify Chang with Misra to reject the claims. It is well established that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desireability of the combination." See MPEP § 2143.01 (citing In re Mills) (emphasis original). Moreover, the Examiner cited no part of Chang or Misra or other reference showing or providing a motivation for the combination in rejecting the claims. Misra only discloses annealing an oxide layer over a substrate, and not an ONO stack as the Examiner suggests.

THE COMBINATION FAILS TO DISCLOSE EACH ELEMENT OF THE CLAIMS

Even if the combination were assumed proper, it is believed that the combination of Chang and Misra fails to meet each element of the claims. For example as stated above, neither Chang nor Misra disclose "annealing the **ONO stack**" as recited in amended independent Claims 2 and 11. Misra simply discloses annealing an oxide layer of a prepared

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substrate. Misra does not disclose "annealing the ONO stack." Arguably, by using the disclosure of Misra and combining it with Chang, the "first layer of silicon dioxide" of the ONO stack in Claims 2 and 11 could be annealed. However, this combination of annealing the first layer of silicon dioxide would still not result in "annealing the **ONO stack**."

Applicants therefore respectfully request reconsideration and allowance of independent Claims 2 and 11, and of their respective dependent claims.

As per Claims 2-10, Misra also fails to disclose the "batch furnace" feature. Misra also fails to disclose the "NO" feature of Claims 3-6 and 12-15.

Additionally, Misra fails to disclose the "carrier gases argon, nitrogen **and** oxygen" feature of Claim 19. Misra discloses "samples annealed in O_2, N_2O, Ar **or** N_2" but not the combination as Claim 19 recites. (See Misra, page 640, § C, first sentence; emphasis added.)

Applicants thus respectfully request withdrawal of the §103(a) rejection, and request reconsideration and allowance of Claims 2-19.

CONCLUSION

In summary, Claims 1-25 were pending in the application. Claims 1-25 were rejected. This response amends Claims 2 and 9-11, and cancels Claims 1 and 20-25. For the above reasons, Applicants respectfully request reconsideration and allowance of Claims 2-19. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned or Bryan Wyman at (408) 453-9200, extension 1345.

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Respectfully submitted,

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Version with markings to show changes made

In the Claims

Please amend Claims 2 and 9-11 as follows:

2. (**Amended**) A method for forming an ONO stack of a floating gate transistor with a first layer of silicon dioxide formed on the floating gate and a layer of silicon nitride formed on the first silicon dioxide layer, comprising:

forming a second silicon dioxide layer by thermally depositing an oxide layer on the silicon nitride layer; and

annealing the ONO stack;

[The method of Claim 1,]wherein the annealing is performed in a batch furnace at temperature range of 800 to 1150 deg Celsius for 300 seconds to 1800 seconds.

9. (**Amended**) The method of Claim 2, wherein the annealing of the ONO stack [layer] is performed in the batch furnace with the gas mixture of 5% to 100% of N_2O with argon as a carrier gas.

10. (**Amended**) The method of Claim 2, wherein the annealing of the ONO stack [layer] is performed in the batch furnace with the gas mixture of 5% to 100% of N_2O with argon, nitrogen and oxygen as a carrier gas.

11. (**Amended**) A method for forming an ONO stack of a floating gate transistor with a first layer of silicon dioxide formed on the floating gate and a layer of silicon nitride formed on the first silicon dioxide layer, comprising:

forming a second silicon dioxide layer by thermally depositing an oxide layer on the silicon nitride layer; and

annealing the ONO stack;

[The method of Claim 1,]wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool at a temperature range of 700 to 1100 deg Celsius for one second to 120 seconds.

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